AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A microcomputer, comprising:

a central processing unit;

a data bus electrically connected to said central processing unit;

~~(a)~~ a cache;

~~(b) a central processing unit, said cache and said central processing unit both being fabricated in one chip; and~~

a command bus electrically connected to said cache and separated from said data bus; and

~~(c)~~ a memory ~~storing commands to be executed by said central processing unit,~~ electrically connected to said command bus, said memory storing an interruption handling routine therein.

2. (Original) The microcomputer as set forth in claim 1, wherein a program is written into said memory by switching memory maps when said microcomputer is turned on.

3. (Currently amended) The microcomputer as set forth in claim 1, wherein said memory ~~is comprised of~~ comprises a command random access memory. ~~(RAM).~~

4. (Currently amended) A microcomputer, comprising:

first, second, third, and fourth buses;

~~(a)~~ a central processing unit;

~~(b)~~ a bus controller electrically connected to said central processing unit through ~~a~~ said first bus;

~~(c)~~ a command cache electrically connected to said central processing unit through ~~a~~ said second ~~bus, and~~ bus and to said bus controller through ~~a~~ said third bus; and

~~(d)~~ a command memory electrically connected to said second bus through ~~a~~ said fourth bus, ~~and~~ for storing an interruption handling routine therein.

5. (Currently amended) The microcomputer as set forth in claim 4, further comprising fifth, sixth, and seventh buses; and a memory controller electrically connected to said bus controller through ~~a~~ said fifth ~~bus, to~~ bus and to said command memory through ~~a~~ said sixth bus, and adapted to be connected to an external memory through ~~a~~ said seventh bus.

6. (Currently amended) The microcomputer as set forth in claim 5, wherein, when said memory controller is connected to the external memory through said seventh bus, said central processing ~~unit, if~~ unit is responsive to said command cache ~~stores~~ storing a command to be executed by said central processing unit, ~~reads~~ to read said command out of said command ~~cache, and executes~~ cache and to execute the thus read-out command, and ~~if~~ said central processing unit is further responsive to said command cache ~~does~~ not ~~store~~ storing a command to be executed by said central processing unit, ~~reads~~ to read a command out of ~~said~~ the external ~~memory, and executes~~ memory and to execute the thus read-out command.

7. (Currently amended) The microcomputer as set forth in claim 4, wherein said central processing unit ~~reads~~ is responsive to an interruption, to read a command out of said command ~~memory, and executes said~~ memory and to execute the interruption handling ~~routine, when interruption occurs~~ routine.

8. (Original) The microcomputer as set forth in claim 4, further comprising an external terminal electrically connected to said central processing unit, and wherein a region in which said command memory is to be arranged is designated through said external terminal.

9. (Currently amended) The microcomputer as set forth in claim 8, wherein said external terminal can be operated ~~even~~ while said central processing unit is in operation.

10. (Original) The microcomputer as set forth in claim 4, further comprising an external terminal electrically connected to said central processing unit, and wherein memory maps are switched through said external terminal.

11. (Original) The microcomputer as set forth in claim 4, further comprising an internal register, and wherein memory maps are switched by said internal register.

12. (Currently amended) The microcomputer as set forth in claim 4, wherein said memory ~~is comprised of~~ comprises a random access memory. ~~(RAM).~~

13. (New) The microcomputer as set forth in claim 1, wherein said cache comprises a command cache.

14. (New) The microcomputer as set forth in claim 1, further comprising a further bus adapted to be connected to an external memory storing a program to be executed by said microcomputer.

15. (New) The microcomputer as set forth in claim 1, further comprising an external terminal electrically connected to said central processing unit, and wherein a region in which said memory is to be arranged is designated through said external terminal.

16. (New) The microcomputer as set forth in claim 15, wherein said external terminal can be operated while said central processing unit is in operation.

17. (New) The microcomputer as set forth in claim 1, further comprising an external terminal electrically connected to said central processing unit, and wherein memory maps are switched through said external terminal.

18. (New) The microcomputer as set forth in claim 1, wherein said central processing unit is responsive to an interruption, to read a command out of said memory and to execute the interruption handling routine.